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219.40605X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): **Scot A. KELLAR et al.**

Serial No.: **10/066,643**

Filed: **February 6, 2002**

For: **WAFER BONDING FOR THREE-DIMENSIONAL (3D) INTEGRATION**

Group: **2811**

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.97 & §1.98

Assistant Commissioner of Patents
Washington, D.C. 20231

May 6, 2002

Sir:

In the matter of the above-identified application, Applicants are submitting herewith copies of the documents listed in the attached form equivalent to Form PTO-1449 for the Examiner's consideration.

This information disclosure statement is being submitted within three months of the filing date.

Each of the documents listed on the attached form equivalent to Form PTO-1449 is in the English language.

It is respectfully requested that this information disclosure statement be considered by the Examiner.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (219.40605X00) and please credit any excess fees to such deposit account.

Respectfully submitted,

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Form PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DKT. NO.	SERIAL NO.
		219.40605X00	10/066,643
	INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	APPLICANT: Scot A. KELLAR et al.	
		FILING DATE: February 6, 2002	GROUP: 2811

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date
	AA						
	AB						
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	AH						
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FOREIGN PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	AM							
	AN							
	AO							
	AP							
	AQ							
	AR							
	AS							
	AT							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	AU	"Ultra Thin Electronics for Space Applications", 2001 Electronic Components and Technology Conference, 2001 IEEE
	AV	"Copper Wafer Bonding"; A. Fan, A. Rahman, and R. Reif; Electrochemical and Solid-State Letters, 2 (10) 534-536 (1999)
	AW	"Face to Face Wafer Bonding for 3D Chip Stack Fabrication to Shorten Wire Lengths", June 27-29, 2000 VMIC Conference 2000 IMIC – 200/00/0090(c)
	AX	"InterChip Via Technology for Vertical System Integration", Fraunhofer Institute for Reliability and Microintegration, Munich, Germany; Infineon Technologies AG, Munich, Germany; 2001 IEEE
	AY	
	AZ	

Examiner	Date Considered